Electronic Version
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Claims

[c1] 1. A method of fabricating a non-volatile memory cell, comprising:
forming a bottom dielectric layer on a substrate;
forming a charge trapping layer on the bottom dielectric layer;
patterning the charge trapping layer, for forming a trench exposing a portion of the bottom dielectric layer;
forming a top dielectric layer over the substrate, covering the charge trapping layer and the exposed bottom dielectric layer;
forming a conductive layer over the substrate, covering the top dielectric layer;
patterning the conductive layer, the top dielectric layer, the charge trapping layer and the bottom dielectric layer, for forming a stacked structure, wherein a width of the stacked structure is larger than a width of the trench; and
forming source/drain regions in the substrate adjacent to edges of the stacked structure.

[c2] 2. The method of fabricating a non-volatile memory cell of claim 1, before forming the source/drain regions in

the substrate adjacent to the sidewalls of the stacked structure, further comprising:
forming a plurality of lightly doped regions in the exposed substrate; and
forming a plurality of spacers on the sidewalls of the stacked structure.

[c3] 3. The method of fabricating a non-volatile memory cell of claim 1, wherein the step of patterning the conductive layer, the top dielectric layer, the charge trapping layer and the bottom dielectric layer comprises aligning the trench to a center of the stacked structure.

[c4] 4. The method of fabricating a non-volatile memory cell of claim 1, wherein the step of forming the bottom dielectric layer comprises forming a silicon oxide layer on a surface of the substrate by a thermal oxidation process.

[c5] 5. The method of fabricating a non-volatile memory cell of claim 1, wherein the step of forming the charge trapping layer comprises forming a silicon nitride layer on the bottom dielectric layer by a chemical vapor deposition process.

[c6] 6. The method of fabricating a non-volatile memory cell of claim 1, wherein the material of the conductive layer

comprises polysilicon.

[c7] 7. The method of fabricating a non-volatile memory cell of claim 1, wherein the material of the charge trapping layer is selected from a group consisting of silicon nitride, tantalum oxide, $SrTiO_3$ and hafnium oxide.

[c8] 8. A method of fabricating a non-volatile memory cell, comprising:
forming a bottom dielectric layer, a charge trapping layer, a first top dielectric layer and a mask layer on a substrate sequentially;
etching the mask layer for forming a first trench exposing a portion of the first top dielectric layer;
forming a plurality of first spacers on sidewalls of the first trench;
using the first spacers as an etching mask and etching the first top dielectric layer and the charge trapping layer for forming a second trench;
removing the first spacers;
forming a second top dielectric layer over the substrate, covering surfaces of the second trench and the first trench;
forming a conductive layer in the first trench and the second trench;
removing the conductive layer and the second top dielectric layer outside of the first trench and the second

trench for exposing the mask layer;
removing the exposed mask layer;
using the conductive layer as a mask, removing the first top dielectric layer, the charge trapping layer and the bottom dielectric layer for forming a stacked structure; and
forming source/drain regions in the substrate adjacent to edges of the stacked structure.

[c9] 9. The method of fabricating a non-volatile memory cell of claim 8, before forming the source/drain regions, further comprising:
forming a plurality of lightly doped regions in the exposed substrate; and
forming a plurality of second spacers on the sidewalls of the stacked structure.

[c10] 10. The method of fabricating a non-volatile memory cell of claim 8, wherein the step of forming the bottom dielectric layer comprises forming a silicon oxide layer on a surface of the substrate by a thermal oxidation process.

[c11] 11. The method of fabricating a non-volatile memory cell of claim 8, wherein the step of forming the charge trapping layer comprises forming a silicon nitride layer on the bottom dielectric layer by a chemical vapor depo-

sition process.

[c12] 12. The method of fabricating a non-volatile memory cell of claim 8, wherein the material of the mask layer comprises silicon nitride.

[c13] 13. The method of fabricating a non-volatile memory cell of claim 8, wherein the material of the first spacers comprise polysilicon.

[c14] 14. The method of fabricating a non-volatile memory cell of claim 8, wherein the material of conductive layer comprises polysilicon.

[c15] 15. The method of fabricating a non-volatile memory cell of claim 8, wherein the material of the charge trapping layer is selected from a group consisting of silicon nitride, tantalum oxide, $SrTiO_3$ and hafnium oxide.

[c16] 16. The method of fabricating a non-volatile memory cell of claim 8, wherein the material of the first top dielectric layer and the second top dielectric layer comprises silicon oxide.

[c17] 17. The method of fabricating a non-volatile memory cell of claim 8, wherein the step of removing the conductive layer and the second top dielectric layer outside of the first trench and the second trench is a chemical

mechanical polishing process or an etch-back process.

[c18] 18. The method of fabricating a non-volatile memory cell of claim 8, wherein the step of removing the mask layer comprises dry etching.